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13. ABSTRACT *(Maximum 200 words)*

The WiTech phase I objectives were to explore the feasibility of A1203 as a buffer layer insulator for GaAs-on-insulator (GOI) technology and as a gate insulator for GaAs-based MISFETs. Specifically, we have:
1) investigated the oxidation process and its effect on active device layers, showing the verlittle or no detrimental effect of the oxidation on the active region can be achieved by using LT-AiGaAs buffer layers.
2) fabricated an measured the performance of GaAs MESFETs with A1203 as a buffer layer insultor demonstrating nearly 50% RF (3 GHz) power added efficiency at low operating bias.
3) fabricated and characterized MIS structures using A1203 as the insulator, showing the challenges and problems associated with using lateral steam-oxidation for producing a gate insulator.

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WiTech

Final Technical Report
May 11, 1998
Low Power GaAs Enhancement-Depletion Technology Using Native Al_2O_3 as an Insulator

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Summary of Profect Objectives

The main project objectives of the WiTech phase I effort were to explore the feasibility of Al_2O_3 (formed by the wet oxidation of AlAs epilayers) as a buffer layer insulator for GaAs-on-insulator (GOI) technology and as a gate insulator for GaAs-based MISFETs. Specifically, we have:

(i) investigated the oxidation process and its effect on active device layers, showing that very little or no detrimental effect of the oxidation on the active region can be achieved by using LT-AlGaAs buffer layers.

(ii) fabricated and measured the performance of GaAs MESFETs with Al_2O_3 as a buffer layer insulator demonstrating nearly 50% RF (3 GHz) power added efficiency at low operating bias.

(iii) fabricated and characterized MIS structures using Al_2O_3 as the insulator, showing the challenges and problems associated with using lateral steam-oxidation for producing a gate insulator.

Also, through a subcontract to Scientific Research Associates, Inc. (SRA), a windows-based user interface and three-dimensional plotting routine has been developed to run software code that is capable of simulating bias and time dependent current, carrier concentration, and electrostatic potential profiles in two-dimensional, three-terminal, multi-layer semiconductor structures with native oxides.

Project Results

A: Study of oxidation rates

Figure 1(a) shows a schematic of one of the samples used to study the wet oxidation rates of $Al_{0.98}Ga_{0.02}As$ layers. The ternary with ~2% Ga is used rather than the binary AlAs as the latter is known to be structurally unstable after oxidation. The growth was done by MBE. First, an LT-$Al_{0.3}Ga_{0.7}As$ layer is grown at 250 °C and annealed in-situ at 550 °C for ~2 minutes. This layer is used as an "arsenic-gettering" layer based on earlier work at UCSB. The rest of the growth is done at 580 °C. Note that the structure contains two separate regions suitable for lateral oxidation, one below and one above a doped GaAs channel. The lower oxidation region consists

of 50 nm $Al_{0.98}Ga_{0.02}As$ with a graded set-back layer. The upper oxidation region is 40 nm $Al_{0.98}Ga_{0.02}As$ with a grade and an $Al_{0.7}Ga_{0.3}As$ etch stop layer. The doped GaAs channel is 200 nm thick with a total sheet charge of 5×12 cm^{-2}, confirmed by Hall measurements.

We characterized the lateral oxidation rates for the upper and lower $Al_{0.98}Ga_{0.02}As$ layers. Oxidation was performed in a tube furnace under steam supplied by flowing N_2 gas through a deionized water bath. Only one cladding layer was oxidized at a time: the upper cladding layer was completely etched away from the sample prior to etching a mesa to expose the lower cladding layer, which conversely was not exposed during oxidation of the upper cladding layer. In all cases, we deposited a protective $Si0_2$ cap (100 nm thick) on the sample surface to prevent unintentional vertical oxidation. As shown in Figure 1(b), the lateral oxidation rates were essentially the same for each layer and they increased with the oxidation temperature. For typical FET devices discussed below, the required lateral oxidation is ~30 μm, which corresponds to an oxidation time of ~40 min and ~20 min at 420°C and 450°C, respectively.

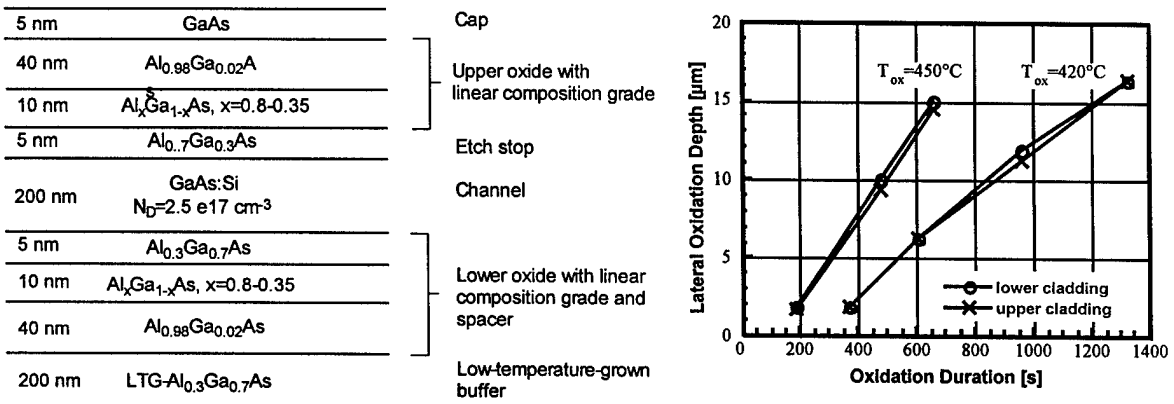

Figure 1: (a) Schematic layer diagram of WiTech GOI/MISFET device structure (sample # 971022C) used to study lateral oxidation rates. (b) Measured lateral oxidation rates of upper and lower $Al_{0.98}Ga_{0.02}As$ layers at 420°C and 450°C.

B: Effects of oxidation on adjacent channel

Using the same growth structure shown in figure 1(a), we performed Hall measurements to investigate the channel mobility and sheet concentration before and after the oxidation process. The width of the mesa-defined Hall bar was 20 μm, and the oxidation time was chosen so that

the oxidation fronts just met in the center of the Hall bar, based on the oxidation rates in figure 1(b). Following the lateral oxidation, undoped capping layers were selectively wet-etched from the contact pad areas. Then AuGe was deposited and annealed at 400°C to make Ohmic contacts to the channel.

As shown in figure 2, significantly different behavior was observed depending on whether the oxidation layer was above or below the channel. For the oxide layer below the channel, the carrier concentration decreases following oxiation and the decrease being larger at the higher oxidation temperature. Note, however, that the channel mobility is not effected by the oxidation. Taken together, these data suggest that the Fermi level at the channel/oxide interface is being pinned but no traps are diffusing into the channel itself during the oxidation process. This is not the case for a different (similar) sample with a LT-GaAs buffer layer. In that case, both the carrier concentration and the mobility drop following oxidation. The reason for the improvement when using an LT-$Al_{0.3}Ga_{0.7}As$ buffer is not clear but it may be related to an increased roughness of the LT-$Al_{0.3}Ga_{0.7}As/Al_{0.98}Ga_{0.02}As$ interface heloing to capturing any excess As that is a by-product of the oxidation process. As discussed below, this issue of preventing oxidation-related traps in the channel is critical to the performance of GOI MESFETs.

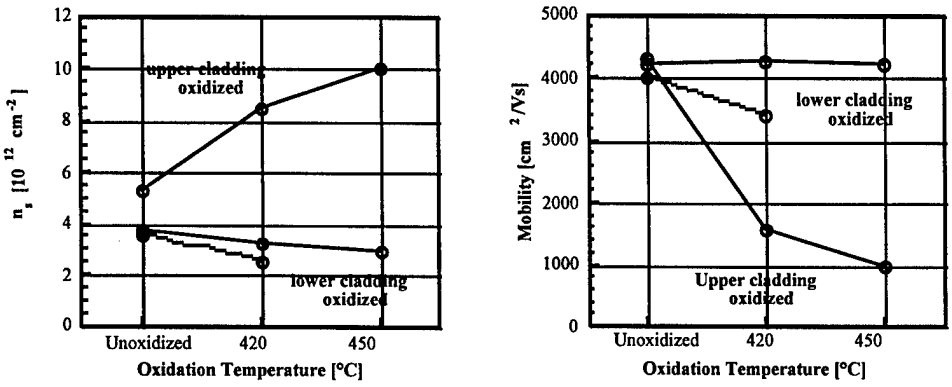

Figure 2: Effect of oxidation of cladding layers on the apparent channel sheet density and mobility. Solid lines are for sample # 971022C (LT-AlGaAs buffer layer); dashed lines are for sample # 970717A (LT-GaAs buffer layer).

In the case of the oxide layer above the channel the carrier concentration appears to increases dramatically following oxidation, while the channel mobility decreases (the inverse of their product, i.e. the sheet resistance, increases). Indeed, following oxidation the carrier

concentration exceeds the total dopant concentration - a remarkable result. Based on C-V measurements (discussed below), this is effect is not real. Instead, it is likely that the oxidized cap layer (or the interface) contains such high density of traps that a parallel hopping conduction path is being formed. Due to the small Hall effect for hopping conduction, this leads to an erroneously high(low) sheet density(mobility).

C: GOI MESFET results

The first GOI MESFET design was based on the work done at UCSB and is schematically illustrated in Figure 3. The growth of this layer preceded the Hall measurements just discussed so its buffer layer was LT-GaAs layer grown at 240 °C rather than LT-AlGaAs. The rest of the growth is done at 580 °C. The oxidation region consists of $Al_{0.98}Ga_{0.02}As$ with a grade and $Al_{0.3}Ga_{0.7}As$ channel set-back layer. The GaAs channel is 200 nm thick with a total sheet charge of 4×12 cm^{-2}, confirmed by Hall measurements. There is an $Al_{0.3}Ga_{0.7}As$ channel etch stop layer and InGaAs ohmic contact layers. The top layers are to prevent the contact layers from seeing any oxidation.

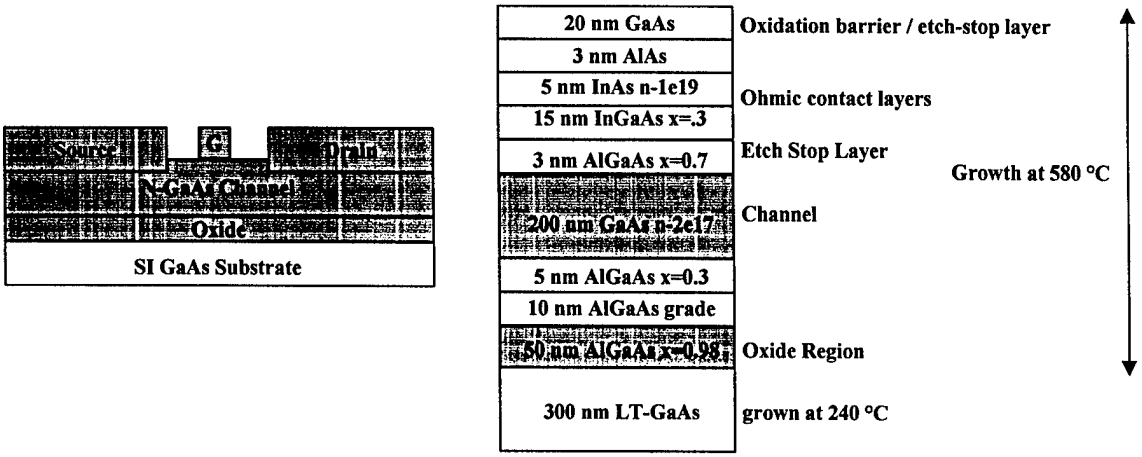

Figure 3: Schematic of and layer diagram of first WiTech GOI device. InGaAs is used for a contact layer, x=0.98 AlGaAs is used for oxidation, and LT-GaAs is used as an "arsenic sink".

The device fabrication is straightforward. First, the mesa is etched to the LT-GaAs layer by selective wet etching. Lateral steam oxidation is then performed at 420 °C until the channel is

completely oxidized. Then the cap layers are selectively wet-etched and the ohmic contacts are deposited and annealed. Finally, the gate region is recess etched to the channel by selective wet etching and the gate is deposited. We tested devices with and without oxidation.

The *I-V* curves of the devices before and after oxidation are shown in figure 4. Before oxidation the maximum current level is ~600 mA/mm. The FETs show a "soft" current saturation as the device nears pinch-off. We believe this is due to traps in the AlGaAs layers, indicating poor initial material quality. The knee voltages at high currents are also high due to a processing error in this sample that resulted in poor ohmic contacts.

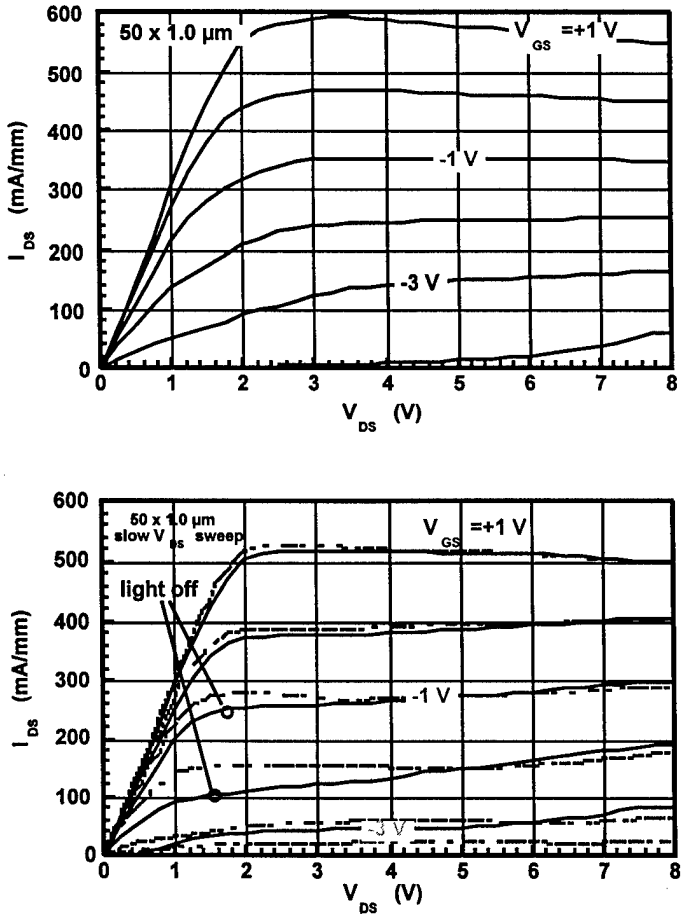

Figure 4: (a) IV curves of as-grown MESFET. The "soft knee" is due to trapping in the AlGaAs, indicating poor material quality. (b) IV curves of GOI MESFET. The device shows ~15% less maximum current and the presence of interface traps is evident from the light sensitivity.

Several differences are present in the oxidized FET IV curves, as shown in figure 4(b). After oxidation, the "soft" knee voltage problem is reduced, verifying that the unoxidized AlGaAs is the culprit. The maximum current level drops to about 520 mA/mm, roughly 15% less than the unoxidized sample, which is consistent with the Hall measurements discussed above. Also, at low currents, bumpy features and a poor output conductance are seen. These effects are reduced in the presence of strong illumination.

Figure 5 shows the transconductance curve for the oxidized sample. A maximum transconductance of 130 mS/mm is obtained with the light on. Also, the curve is relatively flat over a 3 volt range. However, the transconductance is compressed at larger gate voltages. All of the data suggest the presence of traps at the oxide interface or that are present in the $Al_{0.3}Ga_{0.7}As$ spacer layer after oxidation.

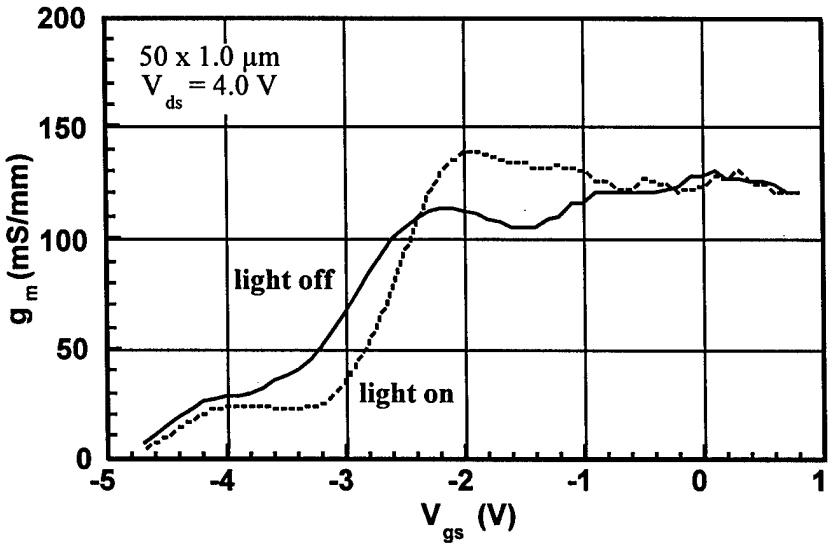

Figure 5: Transconductance curves of oxidized GOI MESFET. The curve is relatively flat over a 3 volt swing but shows compression at larger gate voltages due to interface traps.

Figure 6 shows the RF power data at 4.0 V drain bias for the GOIFET. The data was taken on an ATN load-pull system at 3.0 GHz with only single harmonic tuning. The device is biased in a class AB mode of operation close to pinch-off at an initial drain current bias of 2.2 mA (22 mA/mm). This device had a maximum power added efficiency (PAE) of 49% at a power density of 137 mW/mm, even with the traps in the channel. The efficiency should be higher at lower

frequencies since the gate length of this device is only 1.5μm. The data suggests that the GOI MESFET structure is a device capable of high efficiency at low bias, making it attractive for low power consumption, wireless transmission applications. Minimization of the channel traps present after oxidation will increase the performance of these devices.

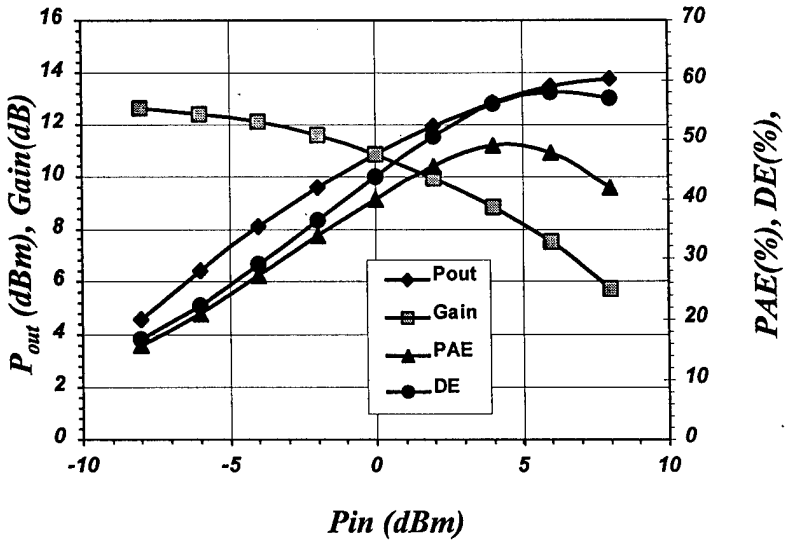

Figure 6: RF power and efficiency data for a 100μm wide GOIFET biased at 4.0 V drain bias. The data is taken at 3.0 GHz with single harmonic tuning in class AB mode.

As shown above, a LT-AlGaAs buffer layer, instead of a LT-GaAs layer can alleviate most of the channel depeletion. WiTech's second generation GOIFET therefore incorporated a LT-AlGaAs buffer. Unfortunately, these devices had very low current levels due to MBE growth problems associated with this particular sample and therefore had poor RF performance. The growth and performance of these LT-AlGaAs based structures will be optimized in phase II of this program.

D: Characterization of Al_2O_3 in a MISFET structure

In addition to buffer layer insulators, we also investigated the feasibility of using the oxide as a gate insulator. There are several issues associated with the use of a steam-oxidized gate insulator in a MISFET that we decided would be more efficiently studied by first fabricating and characterizing simpler devices. Foremost, is characterizing the electrical properties of the oxide which most directly impact the operation of a MISFET - namely (1) leakage current, (2)

breakdown, and (3) density of trap states. To do so, we have performed current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements on diodes incorporating a native Al_2O_3 oxide layer.

We fabricated Shottky diodes on a MISFET-like epilayer structure using standard photolithography. Following the mesa etch, the 500 Å $Al0_{.98}Ga_{.02}As$ layer was laterally oxidized in steam at 420°C. We used several size diodes to investigate the effect of over-oxidation, i.e. continuing to oxidize the layer beyond the time needed for the oxidation fronts from either side of the mesa to meet. Then we deposited AuGe/Ni/Au Ohmic contacts on the channel, which were subsequently alloyed at 410°C for 30 s. (Despite the thin 100 Å GaAs cap, this thermal treatment had no apparent effect on the mechanical stability of the oxide layer). We then selectively etched way the GaAs cap layer (using a citric acid/hydrogen peroxide based etch) and deposited a Ti/Au Schottky contact directly on the native oxide.

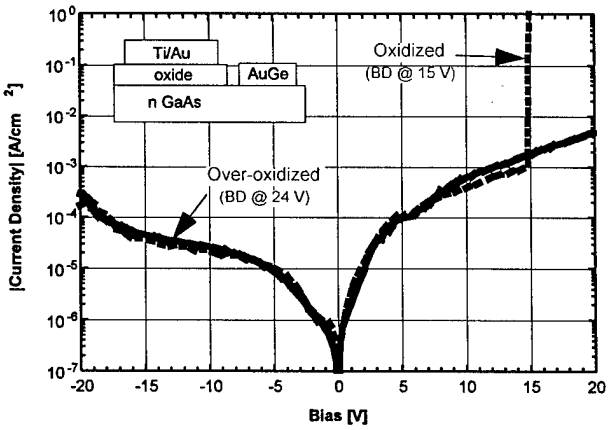

Figure 7. Typical current-voltage characteristics for diodes with just- and over-oxidized (twice as long) $Al_{0.98}Ga_{0.02}As$ layer. Oxidation was at 420 °C. A schematic device structure is also shown.

Figure 7 shows representative room temperature *I-V* curves for MOS diodes in which the $Al_{0.98}Ga_{0.02}As$ layer is just oxidized and for diodes in which the oxidation occurred for twice as long. Under reverse bias conditions, we observe no appreciable difference. In both cases the diodes exhibit a weak bias dependence with a soft, non-destructive "breakdown" at ~-25V. the leakage current increases more rapidly in forward bias, again with no appreciable difference up to moderate voltages. However, the just-oxidized diodes break down catastrophically at ~15 V,

compared to ~24 V for over-oxidized devices. Given that the current density at breakdown is quite low when averaged over the entire contact area, the breakdown is probably of a filamentary nature associated with local, microscopic areas of incomplete oxidation. Unfortunately, if we compare the reverse bias leakage current in figure 6 with a conventional GaAs Schottky diode we find that our native oxide layer does *not* lead to the desired reduction. This indicates that the oxide is not acting as a good insulator, only a large series resistance which can easily support a current comparable to the (small) thermionic emission current over a Ti/Au-GaAs Schottky barrier. The fact that this is not dependent on the duration of the oxidation suggests this is not due to under-oxidation but is inherent to our present device process. It is not clear whether different oxidation conditions and/or additional steps (such as annealing) can eliminate the leakage through the oxide but this is one key issue that will need to be addressed in the future.

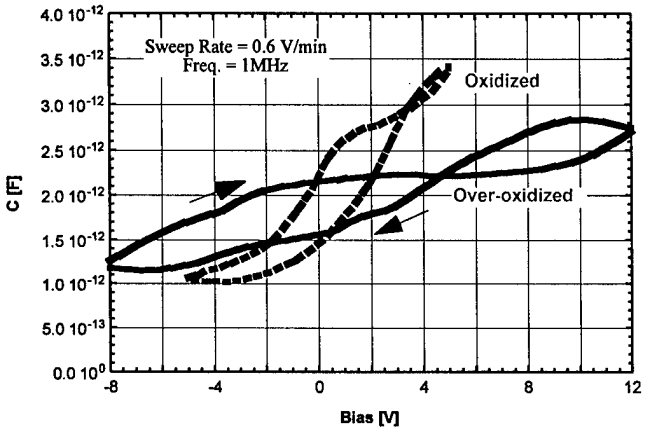

Figure 8. High frequency *C-V* curves for native oxide GaAs/Al_2O_3/Au MOS diodes

A second property of the oxide-semiconductor interface that is critical to the performance of a MISFET is how well the channel in the semiconductor can be modulated by a bias applied to the gate metal. Briefly, the capacitance of our diodes is largely determined by the depletion width of the underlying doped channel and its bias dependence mirrors the modulation of the channel width one would observe in a MISFET fabricated from a similar structure. Figure 8 shows representative results of high frequency (1 MHz) *C-V* measurements. The capacitance changes considerably with bias, particularly in reverse bias (depleting the channel) but the *C-V* curves are stretched out in bias compared to a theoretical curve assuming a perfect oxide. There is also a

pronounced dispersion depending on the direction of the bias sweep. Both of these results indicate the presence of traps either in the oxide or at the channel/oxide interface. Assuming interface traps and an oxide relative dielectric constant of 3, the data are consistent with an interface trap density near the GaAs midgap of $\sim 0.8\times10^{12}$ cm^{-2} and $\sim 3\times10^{12}$ cm^{-2} in the just-oxidized and over-oxidized sample, respectively. Although we do see an increase the capacitance with positive applied bias in these samples, which is equivalent to enhancing the channel width in a MISFET, it is not possible to achieve steady state accumulation conditions at the oxide/channel interface due to the leakage current through the oxide layer described above. In its present status, therefore, the native oxide is not suitable to use as the gate insulator in a GaAs-based MISFET.

E. Software for simulation of native-oxide three terminal devices.

SRA has developed a windows-based user interface and three-dimensional plotting routine to run software code that is capable of simulating bias and time dependent current, carrier concentration, and electrostatic potential profiles in two-dimensional, three-terminal, multi-layer semiconductor structures with native oxides.

Specifically, three types of three-terminal structures can be simulated using the current software. All structures have three base layers, a substrate, a buffer layer, and a channel region. The first structure consists of a gate, source, and drain electrode on top of the channel layer. The second structure consists of a gate on top of the channel and source and drain contacts that are embedded within the channel region. The third structure, shown schematically in figure 9, has the three electrodes on the channel surface, but includes cap layers that can be used to simulate recessed gate or passivated structures.

The windows-based interface allows the user to define devices, set up convergence criteria, and create two and three-dimensional plots of the output. Figure 10 shows a representation of the windows-oriented user interface.

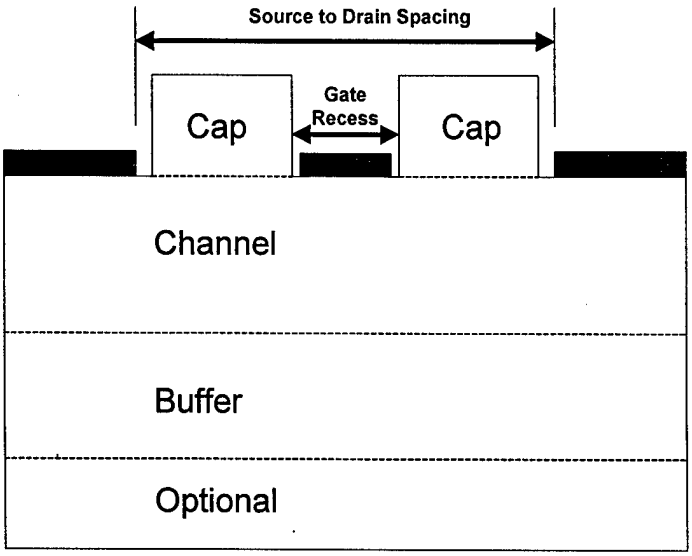

Figure 9: Structure capable of simulating recessed gates or pasivated surfaces.

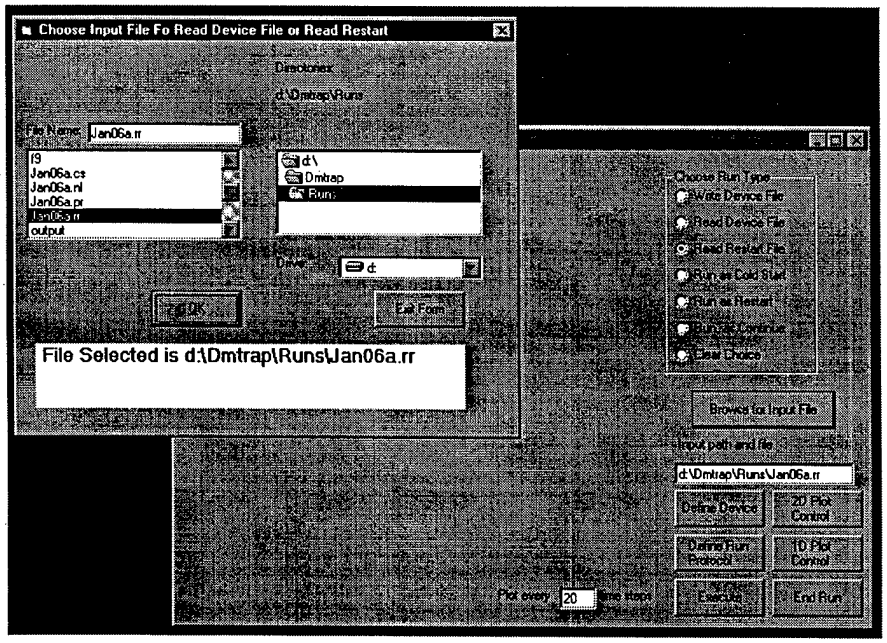

Figure 10: Example of the windows-oriented user interface.

The main feature of the software package are the results obtained from device simulation. In order to evaluate the plotting routines and the software output, the carrier concentration and potential profiles were calculated for a GaAs n-channel MESFET on a lightly-doped p-type buffer layer. Figure 11 shows the three-dimensional plots of the free-electron concentration (log scale, relative to the background concentration of 1e17 cm^{-3} in the channel) in the device under zero drain bias and a 0.75 V Shottky barrier over the gate region. Figure 12 shows the electrostatic potential (relative to thevacuum level; i.e. zero bias gives a potential of -4.1 V for GaAs) for the same structure. The plots can be arbitrarily scaled and rotated for different perspectives by the user. The software can also produce line plots for a given x or y position. Figure 13 shows a line plot, at y = 0.5 μm, of the free electron concentration under the gate. These plotting features ease the evaluation of the device under study.

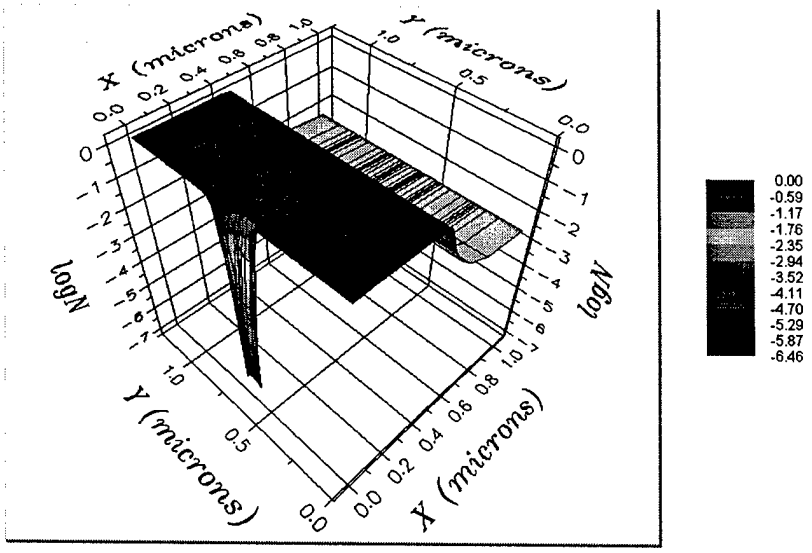

Figure 11: Three dimensional plot of free electron concentration in the n-channel MESFET.

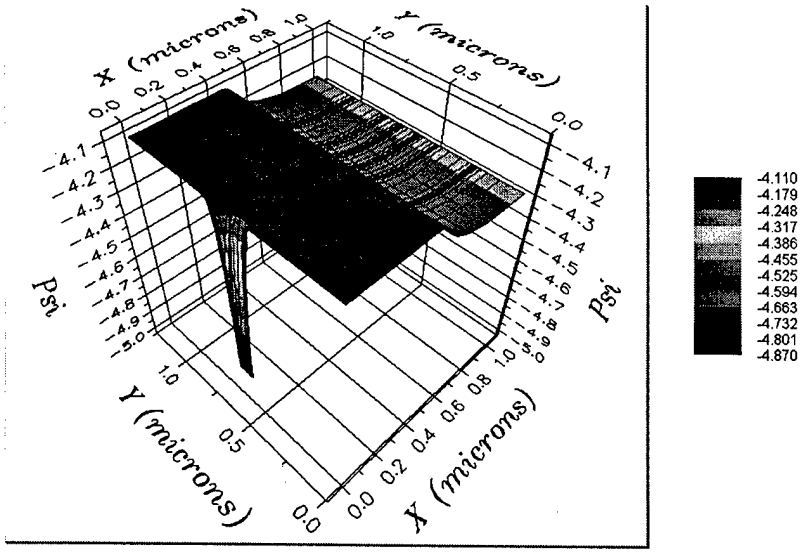

Figure 12: Three dimensional plot of electrostatic potential in the n-channel MESFET.

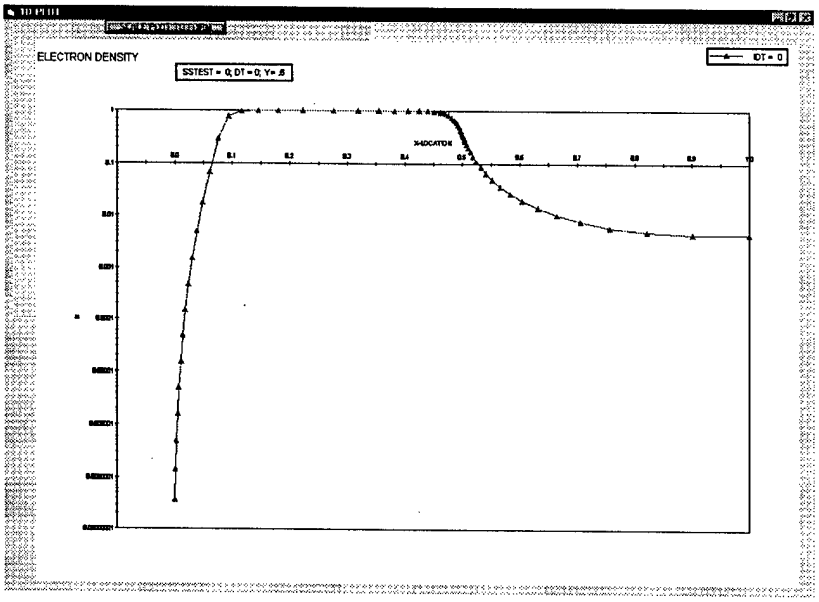

Figure 13: Line plot, at y=0.5 μm, of electrostatic potential in the n-channel MESFET.

Summary

In conclusion, we have demonstrated the feasibility of using selective lateral steam oxidation to produce GOIFETs. We have shown that using LT-AlGaAs as the buffer layer underneath the oxidizing layer minimizes the charge and mobility reduction in the active region of a GOI based device. Using this technology we produced GOIFETs that have nearly 50% power added efficiency at only 4.0 V drain bias, demonstrating the feasibility of this technology for use in the hand-held wireless communications arena. We have also shown that the oxide technology requires significant development for producing MISFET structures that use the lateral oxide as a gate insulator. Finally, a windows-based user interface and plotting routine were developed for native-oxide based three-terminal device simulation software. All of the experimental work for this program was carried out by Dr. James Ibbetson, Dr. Brian Thibeault, and Dr. Yi-Feng Wu of WiTech. The software development was all done by SRA under the supervision of Dr. Harold Grubin.